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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,794	10/06/2004	Kuo-Yang Sun	OSEP0009USA	5793

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 01/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,794	SUN ET AL.	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 10-16* is/are rejected.

7)☒ Claim(s) *3,4 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a semiconductor device that is solder bonded to a set of leads that contain a recession and where a passive device is also bonded to a second set of leads which also contain recessions and a die pad electrically connected to ground and to a semiconductor device must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 13, 15, & 16 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 3,436,818 Merrin et al.

2. Referring to claim 1, a package structure comprising: a lead frame, (Figure 5 #12), having a plurality of first leads, (Figure 5 #12), each of which includes a first recession, (Figure 5 #16); at least a semiconductor chip, (Figure 5 #15 & Col. 4 Lines 44-45); and a plurality of first solder joints, (Figure 5 #24), respectively positioned in the first recessions, (Figure 5 #16), for connecting the semiconductor chip, (Figure 5 #15), to the lead frame, (Figure 5 #12).

3. Referring to claim 2, a package structure, wherein the lead frame, (Figure 5 #12), further comprises a plurality of second leads, (Figure 5 #12), each of which includes a second recession, (Figure 5 #16).

4. Referring to claim 13, a package structure comprising a lead frame, (Figure 5 #12), having a plurality of first leads, (Figure 5 #12), wherein at least two of the first leads, (Figure 5 #12), comprises a first recession, (Figure 5 #16); at least a passive device, (Figure 5 #15 & Col. 4 Lines 44-45), wherein each output of the passive device, (Figure 5 #15), is respectively positioned in the first recession, (Figure 5 #16); and a plurality of first solder joints, (Figure 5 #24), respectively positioned in the first recessions, (Figure 5 #16), for connecting the passive device, (Figure 5 #15), to the lead frame, (Figure 5 #12).

5. Referring to claim 15, a package structure of claim 13 wherein the passive device, (Figure 5 #15 & Col. 4 Lines 44-45), is an electrical resistor, a capacitor, or an inductor.

6. Referring to claim 16, a package structure of claim 13 wherein the first solder, (Figure 5 #24 & Col. 5 Lines 25-26), joints are comprised of tin or tin alloy.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,608,375 Terui et al. in view of U.S. Patent No. 3,436,818 Merrin et al.

7. Referring to claim 13, a package structure comprising a lead frame, (Terui et al Figure 7, 8A-B #305 & Merrin et al Figure 5 #12), having a plurality of first leads, (Terui et al Figure 7, 8A-B #305 & Merrin et al Figure 5 #12), wherein at least two of the first leads, (Terui et al Figure 7, 8A-B #305 & Merrin et al Figure 5 #12), comprises a first recession, (Merrin et al Figure 5 #16); at least a passive device, (Merrin et al Figure 5 #15 & Col. 4 Lines 44-45), wherein each output of the passive device, (Terui et al Figure 7, 8A-B #310 & Merrin et al Figure 5 #15), is respectively positioned in the first recession, (Merrin et al Figure 5 #16 and See ** on the next page); and a plurality of first solder joints, (Terui et al Figure 7, 8A-B #312 & Merrin et al Figure 5 #24), respectively positioned in the first recessions, (Merrin et al Figure 5 #16), for connecting the passive device, (Terui et al Figure 7, 8A-B #310 & Merrin et al Figure 5 #15), to the lead frame, (Terui et al Figure 7, 8A-B #305 & Merrin et al Figure 5 #12).

** Terui et al. teaches all of the claimed matter, but is silent on the first recessions in the leads, but Merrin et al. does. It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Terui et al with the teachings of Merrin et al. because the first recessions in the leads provide a joining plane for the chips and permit the chips to set on the pattern before joining, without tipping and as a result provide a stronger connection and increasing the devices reliability, Merrin et al. Col. 1 Lines 49-51 and Col. 4 Lines 49-51.

8. Referring to claim 14, a package structure of claim 13 wherein the package structure further comprises a semiconductor chip, (Terui et al Figure 7, 8A-B #303), and a plurality of leading wires, (Terui et al Figure 7, 8A-B #304), wherein the semiconductor chip, (Terui et al Figure 7, 8A-B #303), is connected to the leading wires, (Terui et al Figure 7, 8A-B #304).

9. Referring to claim 15, a package structure of claim 13 wherein the passive device, (Terui et al Figure 7, 8A-B #310 and Col. 9 Line 53 & Merrin et al Figure 5 #15), is an electrical resistor, a capacitor, or an inductor.

10. Referring to claim 16, a package structure of claim 13 wherein the first solder, (Terui et al Figure 7, 8A-B #310 Col. 9 Lines 51-52 & Merrin et al. Figure 5 #24 & Col. 5 Lines 25-26 and See *** below), joints are comprised of tin or tin alloy.

*** Terui et al. discloses the claimed invention except for the solder being made out of tin or a tin alloy, but Merui et al does in Col. 5 Lines 25-26. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the solder out of tin or a tin alloy, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 10, & 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,507,120 Lo et al. in view of U.S. Patent No. 3,436,818 Merrin et al.

11. Referring to claim 1, a package structure comprising: a lead frame, (Lo et al Figure 12 #202 & Merrin et al Figure 5 #12), having a plurality of first leads, (Lo et al Figure 12 #202 & Merrin et al Figure 5 #12), each of which includes a first recession, (Merrin et al Figure 5 #16); at least a semiconductor chip, (Lo et al Figure 12 #210 & Merrin et al Figure 5 #15 & Col. 4 Lines 44-45); and a plurality of first solder joints, (Lo et al Figure 12 #218 & Merrin et al Figure 5 #24), respectively positioned in the first recessions, (Merrin et al Figure 5 #16 & See */* below), for connecting the semiconductor chip, (Lo et al Figure 12 #210 & Merrin et al Figure 5 #15), to the lead frame, (Lo et al Figure 12 #202 & Merrin et al Figure 5 #12).

/ Lo et al. teaches all of the claimed matter, but is silent on the first and second recessions in the leads, but Merrin et al. does. It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Lo et al with the teachings of Merrin et al. because the first recessions in the leads provide a joining plane for the chips and permit the chips to set on the pattern before joining, without tipping and as a result provide a stronger connection and increasing the devices reliability, Merrin et al. Col. 1 Lines 49-51 and Col. 4 Lines 49-51.

12. Referring to claim 2, a package structure, wherein the lead frame, (Lo et al Figure 12 #202& Merrin et al Figure 5 #12), further comprises a plurality of second leads, (Lo et al Figure 12 #202 & Merrin et al Figure 5 #12), each of which includes a second recession, (Merrin et al Figure 5 #16 & See */* above).

13. Referring to claim 10, a package structure, wherein the lead frame, (Lo et al Figure 12 #202 & Merrin et al Figure 5 #12), comprises a die pad, (Lo et al Figure 12 #242), connected to the semiconductor chip, (Lo et al Figure 12 #210 & Merrin et al Figure 5 #15), for radiating the heat produced by the semiconductor chip, (Lo et al Figure 12 #210 & Merrin et al Figure 5 #15), by serving as a heat sink, (Lo et al Figure 12 #242).

14. Referring to claim 12, a package structure, wherein the first solder joints are comprised of tin or tin alloy, (Lo et al. Figure 12 #218 & Merrin et al. Figure 5 #24 & Col. 5 Lines 25-26 and See *//* below).

// Lo et al. discloses the claimed invention except for the solder being made out of tin or a tin alloy, but Merrin et al does in Col. 5 Lines 25-26. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the solder out of tin or a tin alloy, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, & 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,984,878 Park et al. in view of U.S. Patent No. 3,436,818 Merrin et al.

15. Referring to claim 1, a package structure comprising: a lead frame, (Park et al Figure 8 #120 & Merrin et al Figure 5 #12), having a plurality of first leads, (Park et al Figure 8 #120 & Merrin et al Figure 5 #12), each of which includes a first recession, (Merrin et al Figure 5 #16); at least a semiconductor chip, (Park et al Figure 8 #240 & Merrin et al Figure 5 #15 & Col. 4 Lines 44-45); and a plurality of first solder joints, (Park et al Figure 8 #241 & Merrin et al Figure 5 #24), respectively positioned in the first recessions, (Merrin et al Figure 5 #16 & See ** below), for connecting the semiconductor chip, (Park et al Figure 8 #240 & Merrin et al Figure 5 #15), to the lead frame, (Park et al Figure 8 #120 & Merrin et al Figure 5 #12).

** Park et al. teaches all of the claimed matter, but is silent on the first and second recessions in the leads, but Merrin et al. does. It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Lo et al with the teachings of Merrin et al. because the first recessions in the leads provide a joining plane for the chips and permit the chips to set on the pattern before joining, without tipping and as a result provide a stronger connection and increasing the devices reliability, Merrin et al. Col. 1 Lines 49-51 and Col. 4 Lines 49-51.

16. Referring to claim 2, a package structure, wherein the lead frame, (Park et al Figure 8 #120 & Merrin et al Figure 5 #12), further comprises a plurality of second leads, (Park et al Figure 8 #120 & Merrin et al Figure 5 #12), each of which includes a second recession, (Merrin et al Figure 5 #16 & See ** above).

17. Referring to claim 10, a package structure, wherein the lead frame, (Park et al Figure 8 #120 & Merrin et al Figure 5 #12), comprises a die pad, (Park et al Figure 8 #110), connected to the semiconductor chip, (Park et al Figure 8 #240), for radiating the heat produced by the semiconductor chip, (Park et al Figure 8 #240), by serving as a heat sink, (Park et al Figure 8 #112 Col. 2 Lines 61-64).

10-13. Referring to claim 11, a package structure, wherein the die pad comprises a ground pad, (Park et al Figure 8 #110 and Col. 2 Lines 61-64), connected to both ground and the semiconductor chip, (Park et al Figure 8 #240).

18. Referring to claim 12, a package structure, wherein the first solder joints are comprised of tin or tin alloy, (Park et al Figure 8 #241 & Merrin et al. Figure 5 #24 & Col. 5 Lines 25-26 and See ** below).

** Park et al. discloses the claimed invention except for the solder being made out of tin or a tin alloy, but Merrin et al does in Col. 5 Lines 25-26. It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the solder out of tin or a tin alloy, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Allowable Subject Matter

19. Claims 3, 4, & 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
1/12/06

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